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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,026	07/26/2001	Gowri Rajaram	UTL 00113	7642

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EXAMINER	
TORRES, MARCOS L	
ART UNIT	**PAPER NUMBER**
2617	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/917,026	RAJARAM, GOWRI	
	Examiner	Art Unit	
	Marcos L. Torres	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-48 and 51-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *54* is/are allowed.

6)☐ Claim(s) *39-48,51-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 8, filed 4-4-07, with respect to objection to claims 51 and 52 have been fully considered and are persuasive. The objection of claims 51-52 has been withdrawn.

2. Applicant's arguments filed 4-4-07 have been fully considered but they are not persuasive.

3. Regarding applicant argument that no motivation has been supplied for the combination Hutchison and Kuroda, the motivation to combine the reference can be found in page 4, lines 13-15 of the prior office action.

4. As to applicant argument that Hutchison and Kay are directed to different fields (since there is no Kay reference in the prior office action, examiner will presume that applicant is referring to Kuroda), both reference are directed to update programming code in devices and link the updated code with the rest of code (Hutchison, see abstract; Kuroda, see col. 1, lines 20-24; col. 4, lines 21-31). Thereby, both references are analogous in the same field of endeavor.

5. Regarding applicant argument that Hutchison is only directed to downloading extension and addition to the system; that characterization in misplaced, Hutchison discloses updating also the main program (see col. 7, lines 30-35).

6. As to applicant argument that the combination Hutchison and Kuroda do not motivate to overwrite a code section; both references motivate to over write a code

section. Hutchison discloses using a erasable programmable read only memory (EEPROM) to save the main program and the features (see col. 3, lines 55-57), and replacing programming section 126 with a new programming section 126 (see col. 7, lines 10-20), that is called overwriting. The pointers are going to be replaced only "if necessary". Therefore it can overwrite to save the main program and alteration to the programs in the same area (see col. 7 lines 30-35; col. 8, lines 20-24. Also Kuroda disclose overwriting (replacing) programming code (see col. 1, lines 20-28).

7. Regarding applicant argument that Hutchison teaches away from overwriting with a new version in fig. 2, since Hutchinson does not describe the process; Please, also see col. 7, lines 10-20.

8. As to applicant suggestion that the combination would not be successful because the memory would fill up; it is within the knowledge of one of the ordinary skill in the art that if there are unused area with old data, it can be overwritten with new data especially in an EEPROM. Moreover, it would be absurd that one of the ordinary skills in the art to fill up the memory because he does not erase the old data in an erasable programmable read only memory. Hutchison clearly discloses that if the programming code 126 needs to be modified is going to replace the same area.

9. Therefore, the combination Hutchison and Kuroda discloses all claim limitations.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 39-47 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hutchison US006449476B1 in view of Kuroda US006457174B1.

As to claim 39, Hutchison disclose a method for updating system software in a wireless communications device (see col. 1, lines 8-11), coping a patch manager code section (program) stored in a nonvolatile memory (ROM) to a volatile memory (RAM) (moving data from ROM to be executed in RAM; shadowing see col. 3, lines 57-64); receiving a broadcasted system software update comprising an update code section (see col. 7, lines 49-53) and a update patch manager (see col. 7, lines 31-35); storing the system software update on a file system section of the nonvolatile memory module (see fig. 1, item 116), overwriting at least a portion of a code section of a plurality of code sections stored in a code storage section of the nonvolatile memory with the code update code section (see col. 7, lines 10-20; col. 8, lines 7-9, 20-35; col. 3, lines 55-57), each code section of the plurality of code section comprising at least one symbol library having a plurality of symbols of related functionality (features)(see col. 5, lines 2-10; fig.

1, 2); updating at least a portion of the patch manager code section of the nonvolatile memory with at least a portion of the update patch manager (see col. 7, lines 31-35), comprising updating a code section address table of the patch manager code section which store a code section identifier and a start address for each code section of the plurality of code sections (see fig. 4, item 174-180; col. 7, line 66 – col. 8, line 35). Hutchinson does not specifically disclose updating a symbol offset address table which stores an offset reference for each symbol of the plurality of symbols in the at least one symbol library of the each code section, the offset reference comprising an offset value derived from the start address of the each code section.

In an analogous art, Kuroda discloses the method of updating a symbol offset address table which stores an offset reference for each symbol of the plurality of symbols in the at least one symbol library of the each code section, the offset reference comprising an offset value derived from the start address of the each code section (see abstract); and overwriting (replacing) data (see col. 1, lines 20-28). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to add this technique to the Hutchison method for better management of the memory resources.

As to claim 40, Hutchinson disclose the method further comprising executing the system software update from the nonvolatile memory, loading the system software update from the patch manager code section and the code storage section within the nonvolatile memory module to a volatile memory component and performing at least one requested action (see col. 5, lines 11-65).

As to claims 41 and 43-44, Hutchinson disclose the method wherein each symbol of the plurality of symbols is associated with a symbol access code (see col. 4, lines 15-22), further comprising: arranging the symbol access code in the corresponding symbol library and repeating the step above (see col. 4, lines 27-36; col. 5, lines 11-61), since the claim does specify the difference between a symbol library and symbol access code, for examining purposes they are the same.

As to claim 42, Hutchinson disclose the method further comprises referencing the symbol access code to calculate an address of a sought symbol, comprising accessing a code section address table and a symbol address table to determine a corresponding code section identifier and accessing the code section address table to determine a start address of the corresponding code section (see col. 6, lines 9-21; col. 4, lines 16-22). Hutchinson does not specifically disclose using an offset address table. In an analogous art, Kuroda discloses a symbol offset address table (see abstract).

Regarding claims 45 and 53 are the corresponding apparatus claims of method claims 39 and 43. Therefore, claims 45 and 53 are rejected for the same reasons shown above.

As to claims 47, Hutchinson discloses the wireless communication device wherein the patch manager code section further comprises (see fig. 1, item 114,115,116): a read-write section (see fig. 1, item 114,115,116): a symbol accessor code section (see fig. 2, item 124,126,128); a symbol accessor address code section (see fig. 3, item 160); and a patch library (see col. 5, lines 2-10).

As to claims 51, Hutchinson discloses the wireless communication device wherein the at least one code storage section comprises at least two code sections (see fig. 1, item 1116,134,136); wherein the received updated code section and the received updates patch manager code section define a system software update, and wherein code section of the at least two code section store at least part of the software update (see col. 5, lines 11-61).

As to claims 46 and 52, Hutchinson discloses the wireless communication device wherein the patch manager code section is configured to control the system software update (see col. 9, lines 7-30).

13. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hutchinson inn view of Kuroda as applied to claim 45 above, and further in view of Shaw 20020026634.

As to claim 48, Hutchison and Kuroda disclose everything as explained above (see claim 45) except for the wireless communication device wherein the patch manager code section is loaded into a volatile memory upon a reset condition. In an analogous art, Shaw discloses for the wireless communication device wherein the patch manager code section is loaded into a volatile memory upon a reset condition (see par. 0024-0026). Therefore, it would have obvious to one of the ordinary skill in the art at the time of the invention to use a reset to upgrade for the simple purpose of initialize with the new code.

Allowable Subject Matter

14. Claim 54 is allowed.

15. The following is an examiner's statement of reasons for allowance: the combination of **all** the features in the update process have not found or fairly suggested in the prior art search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this Office Action should be mailed to:

U.S. Patent and Trademark Office
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Or faxed to:

571-273-8300

for formal communication intended for entry, informal communication or draft communication; in the case of informal or draft communication, please label "PROPOSED" or "DRAFT"

Hand delivered responses should be brought to:

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marcos L. Torres whose telephone number is 571-272-7926. The examiner can normally be reached on 8:00am-6:00 PM alt. Wednesday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, George Eng can be reached on 571-252-7495. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Marcos L Torres
Examiner
Art Unit 2617

mlt

GEORGE ENG
SUPERVISORY PATENT EXAMINER